

ELECTRICAL AND THERMAL BEHAVIOUR OF INNOVATIVE NANOPACKAGING INTERCONNECTS

A. G. Chiariello¹, A. Maffucci² and G. Miano¹

¹DIEL, Università degli studi di Napoli “Federico II”, Via Claudio 21, 80125 , Napoli

²DAEIMI, Università di Cassino, Via Di Biasio 43, 03043, Cassino (FR)

A challenging task for future nanoelectronics technology is given by *nanopackaging*, i.e. the effective capability of complementing the nanometric device features to the circuit boards [1]. Many of the requirements for the nanopackages in terms of mechanical, electrical and thermal behavior still fall in unknown-solution areas. The physical phenomena at nanoscale put limits to the possibility of simply continuing to scale the conventional metal/dielectric systems in the frame of the classical packaging technologies. It is needed an “*unprecedented pace of innovation in new materials, new technology and new system integration techniques*”.

Recently the first examples of successful integration between CNT and CMOS in nanopackaging have been proposed: in [2], vertical CNT bundles are used as bumps for flip-chip interconnects, replacing conventional solder bumps, Fig.1a. In this paper we model the parasitic resistance of short nanopackaging interconnects, comparing the performances of copper and carbon nanotubes with emphasis of the effect of sizes and temperature.

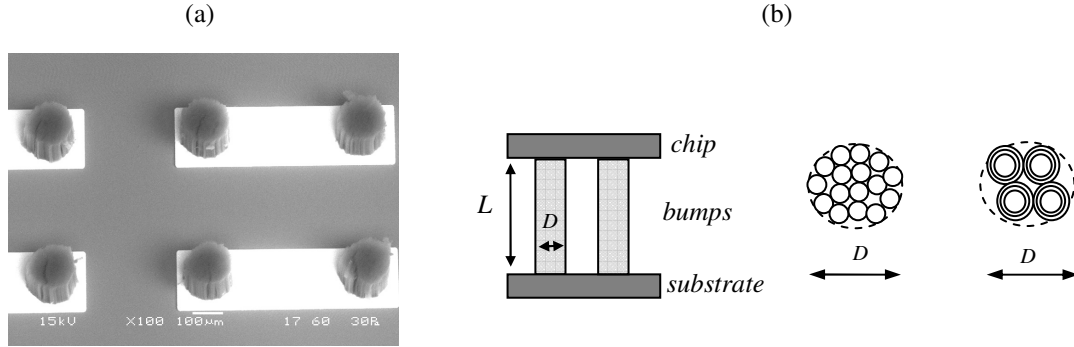


Fig.1. (a) Vertical Carbon Nanotube bundles as flip-chip bumps [2]; (b) schematic of a nanopackage structure with the pillars made by SWCNTs or MWCNTs.

We use a recently proposed model [3], which relates the CNT shell resistivity to the *number of equivalent conducting channels*, expressed as a function of the CNT chirality, diameter D and temperature T . An approximation for this number for a single CNT shell is:

$$M \approx \begin{cases} M_0 & \text{for } D < d_0 / T \\ a_1 D T + a_2 & \text{for } D \geq d_0 / T \end{cases}, \quad (1)$$

being D the shell diameter and T the absolute temperature. The fitting parameters are given in [3]. The resistance R_s of a single CNT shell of length l is modeled by:

$$R_s = \frac{R_0}{M} \left(1 + \frac{l}{2l_{mfp}} \right), \quad (2)$$

where $R_0 = h/2e^2 = 12.9 \text{ k}\Omega$ is the *quantum resistance* and l_{mfp} is the mean free path. In the range $270 \text{ K} < T < 420 \text{ K}$ a simple model for the mean free path is [4]:

$$\frac{1}{l_{mfp}} = \frac{T/T_0 - 2}{bD} \quad (T_0 = 100 \text{ K}, b = 500.) \quad (3)$$

Let us consider the case of a SWCNT. The typical values of D (few nm) are such that it is always $D < d_0/T$. Therefore, the resistance of a bundle of N SWCNTs fed in parallel (assuming 1/3 of them to be metallic) is given by:

$$R = \frac{3R_0}{2N} \left(1 + l \frac{T/T_0 - 2}{2bD} \right). \quad (4)$$

Instead in the case of the MWCNT, the shell diameters are such that $D > d_0/T$, hence the resistance introduced by the i -th shell is:

$$R_i = \frac{R_0}{a_1 D_i T + a_2} \left(1 + l \frac{T/T_0 - 2}{2bD_i} \right). \quad (5)$$

Figure 2a shows that the lowest values of parasitic resistance are obtained by using MWCNT bundles, whereas SWCNT bundle shows performances comparable to copper. All the realizations suffer from the temperature increase, apart from the MWCNT one, for which the increase of the number of conducting channels as temperature increase (see (1)) counteracts the reduction of l_{mfp} predicted by (3), as shown in Fig.2b.

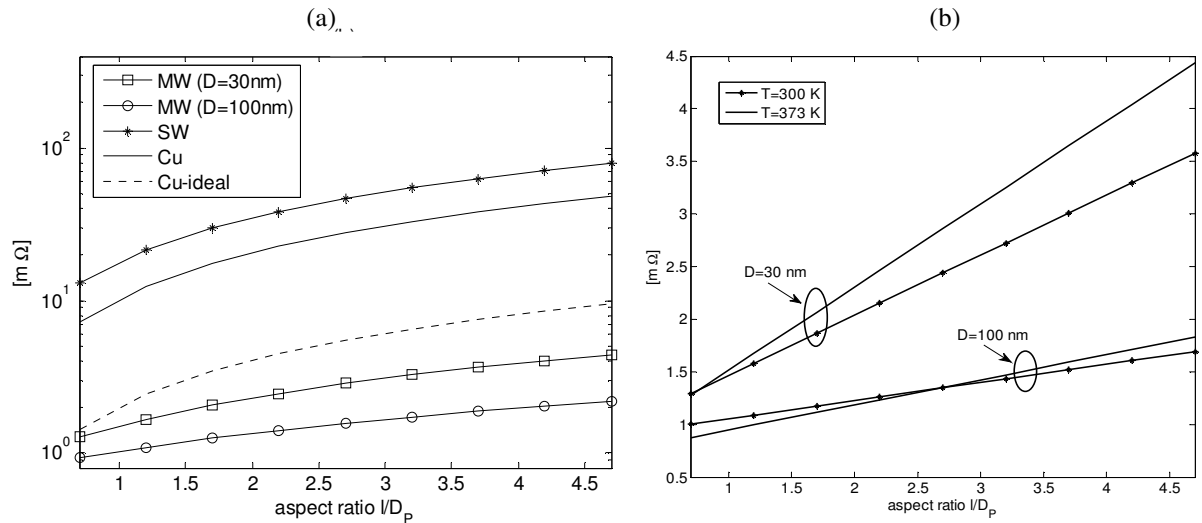


Fig.2. (a) Bump parasitic resistance computed at $T=373\text{K}$, vs aspect ratio: Cu, SWCNTs and MWCNT bundles, (b) Parasitic resistance of two MWCNT bundle realizations of the pillar bump.

References

- [1] Morris, J.E., *Nanopackaging: Nanotechnologies and electronics packaging*, Springer (New-York, 2008).
- [2] Soga I. et al., "Carbon nanotube bumps for LSI interconnect," *Electronic Components and Technology Conf., ECTC* (2008), pp.1390-1394.
- [3] Chiariello, A.G., et al., "Carbon Nanotubes Interconnects for Nanoelectronics Circuits", in *Carbon nanotubes*, IN-TECH (Vienna, Austria, 2010).
- [4] Naeemi, A. and Meindl, J.D., "Performance Modeling for Single- and Multiwall Carbon Nanotubes," *IEEE Trans. on Electron Dev.*, Vol. 55 (2008) pp. 2574-2582.